HETEROGENEOUS INTEGRATION OF CO-EVAPORATED BISMUTH/ANTIMONY TELLURIDE THIN FILMS BASED THERMOELECTRIC HARVESTERS ON FINFET CMOS CHIP

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Abstract: This paper presents the fabrication of bismuth telluride (Bi$_2$Te$_3$) and antimony telluride (Sb$_2$Te$_3$) thin film-based thermoelectric harvesters on silicon-on-insulator (SOI) substrate with FinFET (field-effect transistor) based CMOS (complementary metal oxide semiconductor). These films can be used to integrate planar thermoelectric generators (TEG) or thermoelectric coolers (TEC) directly with CMOS circuits. The thermoelectric films are deposited by co-evaporation through shadow-masks in a post-CMOS process, with improved contact resistance via pre-deposition surface treatments. Transistor performance showed no significant change upon TEG fabrication, indicating CMOS compatibility of the thermoelectric thin film deposition process. A 2.14×2.14-mm$^2$ sized square-shaped planar thermoelectric harvester has been fabricated as a demonstration vehicle and generates 0.67 µW from a temperature gradient of 21 K, with an average open circuit output of 233 µV/K per thermocouple.

Keywords: thermoelectric, bismuth telluride, antimony telluride, CMOS, FinFET, co-evaporation, heterogeneous

INTRODUCTION

Uneven heat distribution in conventional integrate circuits (ICs) can lead to a temperature variation of 5-30°C from one location to another in the same chip [1], which can cause decreased performance and chip failures due to electro-migration and oxide breakdown. An integrated micro thermoelectric (TE) device can be utilized either to harvest energy from the undesired heat, or to reduce the large temperature gradient by cooling the micro-hotspots. Compared to conventional macro-scale thermal management systems, integrated micro TE devices can provide a solid-state solution with appealing advantages of DC operation, low power consumption, smaller package size, quiet operation due to no moving parts [2], and no dependence on a laser source [3], high-pressure gas compressor [4], or refrigerant fluid reservoir [5].

Previous studies on heterogeneous TE integration on CMOS have been limited to conventional materials such as poly-Si [6] or poly-SiGe [7], which have very low thermoelectric figure of merit (0.005-0.061) compared to Bi$_2$Te$_3$/Sb$_2$Te$_3$ (0.34-0.41) [8]. High-quality Bi$_2$Te$_3$ and Sb$_2$Te$_3$ films can be evaporated at ~250°C, and they provide high thermoelectric performance near room temperature due to their high Seebeck coefficient, low electrical resistivity and relatively low thermal conductivity near room temperature [9]. Co-evaporation [10] and sputtering [11] are potentially compatible with CMOS processes, and they provide a good degree of structural order and allow reproducible control over film composition, uniformity, thickness and material properties.

![Fig. 1: Cross-section and top view schematic of a planar thermoelectric energy generator near CMOS.](image)

![Fig. 2: Heterogeneously integrated TEG with Bi$_2$Te$_3$ and Sb$_2$Te$_3$ legs on a FinFET CMOS substrate.](image)
PLANAR TEG DESIGN

The planar TEG is designed in a square-shaped layout with a total of 12 thermocouples in an area of 2.14×2.14-mm² (Figs. 1-2). The width (~100µm) and length (~350µm) of thermoelectric legs is optimized analytically to provide the maximum electrical power output for a fixed thermal power input (Fig. 3). An on-chip resistive (metal) heater and temperature-sensors are placed at the center and circumference of the TEG, in order to create and measure planar thermal gradients across the TE legs to test the efficiency of the harvester in this prototypical device.

POST-CMOS TE FILM DEPOSITION

The 8-inch FinFET CMOS wafer is diced into 25-mm×30-mm sized pieces prior to the TEG process for rapid prototyping and a decreased cost of process characterization. The CMOS process used in this study ends with a TEOS interlayer dielectric (ILD) and a top aluminum metal layer. The planar TEG is fabricated on the TEOS dielectric in the open areas between CMOS devices. The TEG process involves e-beam deposition and lift-off patterning of a metal layer to serve as electrical interconnects, heaters, and temperature sensors. On top of the metal interconnects and TEOS ILD, n-type Bi₂Te₃ (270°C), and p-type Sb₂Te₃ (250°C) are evaporated and in situ patterned through aligned shadow masks. The TE film co-evaporation process was previously characterized to allow precise thickness control, good film adhesion and uniform poly-crystalline morphology [10]. An improved shadow mask process shown in Figure 4, is utilized in this study for higher precision alignment and masking during TE film deposition and patterning. Finally, as an optional process step, the silicon substrate between the hot and cold regions is removed by backside DRIE to increase the thermal isolation across TE legs, although this process step also creates a mechanical vulnerability to external vibration or shocks due to the suspended SiO₂ membrane.

TE film evaporation through shadow masks with 200µm-deep deposition holes enables sufficiently precise alignment and pattern dimensions, however it also results in a decreased deposition rate (Table 1). There is a 45% reduction in deposited TE thickness compared to blanket deposition, and this masking effect is compensated by longer deposition periods (Fig. 5). Minimizing contact resistance is important in integrated thin film TEGs, especially for highly dense structures with small contact areas. A Cr/Au metal layer is preferred in this study due to its non-oxidizing nature, and low contact resistance of $2.0\times10^{-8}$ Ω-m².

Before TE deposition, plasma treatment is performed to clean the deposition surface. This improves the TE-metal interface, decreasing the average resistance of a single thermocouple to ~80Ω from >270Ω (for deposition on untreated surfaces).

Table 1: Effect of the shadow mask (110µm-wide and 200µm-deep deposition holes) on the deposited film thickness.

<table>
<thead>
<tr>
<th>Dep. Film</th>
<th>Blanket Deposition</th>
<th>Thru Shadow Mask</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bi₂Te₃</td>
<td>1.75 µm</td>
<td>0.80 µm</td>
</tr>
<tr>
<td>Sb₂Te₃</td>
<td>1.55 µm</td>
<td>0.70 µm</td>
</tr>
<tr>
<td>Bi₂Te₃</td>
<td>4.00 µm</td>
<td>1.80 µm</td>
</tr>
<tr>
<td>Sb₂Te₃</td>
<td>3.75 µm</td>
<td>1.65 µm</td>
</tr>
<tr>
<td>Dep. Rate (nm/min)</td>
<td>16.3</td>
<td>7.4</td>
</tr>
<tr>
<td></td>
<td>14.9</td>
<td>6.7</td>
</tr>
</tbody>
</table>
The TEG is tested at different applied temperature gradients (ΔT). It provides an average open-circuit output of ~230 μV/K per thermocouple (Table 2). For a ΔT of 21 K, TEG generates 58.5 mV open-circuit voltage, and delivers 0.67 μW to a 1.27 kΩ resistive load. In order to increase the amount of power harvested, the thermal isolation between hot and cold sides should be improved, and the planar/vertical heat flow paths should be specifically designed and optimized for a particular circuit layout.

The integrated NMOS-FinFETs are tested before and after TEG process, and the shift in I-V characteristics of the same device (Fig. 8) is less than the observed die-to-die variation in original transistor performance (Fig. 9). This demonstrates the CMOS-compatibility of the current TEG process which uses co-evaporated Bi$_2$Te$_3$ and Sb$_2$Te$_3$ films. Although Cr/Au metal interconnects are used in the current process, in the future CMOS-compatible metal contacts could be used instead.
CONCLUSION

In this paper, heterogeneous integration of micro thermoelectric devices on a FinFET CMOS fabricated on SOI substrate is demonstrated. A thermoelectric generator is co-fabricated by co-evaporation of bismuth telluride and antimony telluride thin films in a scalable post-CMOS process. Measured transistor performance showed no significant change upon TEG fabrication, indicating the CMOS compatibility of the thermoelectric thin film deposition process. The total resistance of a single thermocouple is reduced to less than 80 Ohms by introducing plasma treatment before deposition, and the average output of one thermocouple is measured as ~230 µV/K. We expect that future improved device architectures based on the presented technology can harvest energy from the on-chip temperature gradients produced by a high-load CMOS chip during operation and convert it back into electrical energy to improve the system power efficiency. Alternatively, the same technology can be used to build integrated thermoelectric coolers to cool certain chip locations for improved electronic/thermal noise.

ACKNOWLEDGEMENT

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REFERENCES


Table 2: Measured TEG results (12 thermocouples, inner heater area = 1.6mm², total TEG area = 3.0mm²)

<table>
<thead>
<tr>
<th>Inner Heater</th>
<th>Outer Sensor</th>
<th>Measured ΔT between sensors</th>
<th>Calculated ΔT across TE legs</th>
<th>Open Circuit TEG Output</th>
<th>V_{OPEN-CIRCUIT} / ΔT / Thermocouple</th>
<th>Power Output to R_{LOAD} = 1.27 kΩ</th>
</tr>
</thead>
<tbody>
<tr>
<td>27.5 °C</td>
<td>25.0 °C</td>
<td>2.5 K</td>
<td>1.3 K</td>
<td>3.83 mV</td>
<td>246 µV/K</td>
<td>2.9 nW</td>
</tr>
<tr>
<td>42.3 °C</td>
<td>31.9 °C</td>
<td>10.4 K</td>
<td>5.5 K</td>
<td>15.16 mV</td>
<td>230 µV/K</td>
<td>45.4 nW</td>
</tr>
<tr>
<td>99.0 °C</td>
<td>59.6 °C</td>
<td>39.4 K</td>
<td>20.9 K</td>
<td>58.53 mV</td>
<td>233 µV/K</td>
<td>676.5 nW</td>
</tr>
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